App. Serial No. 09/737,606 Docket No.: US008082

In the Claims:

Please amend claims 1 and 21 as indicated below. This listing of claims replaces all prior versions.

1. (currently amended) A wafer for fabricating integrated circuits using a stepper, said wafer comprising:

a first region of the wafer, the first region having four sides and having a scribe line along each of the four sides of the first region; and

four alignment targets disposed within said scribe line;

wherein one alignment target is located on each of the four sides of the first region wherein a first alignment target on a first side of the first region and a second alignment target on a second side of the first region opposing said first side are located in mirror-image positions, and <u>further including an overlaywherein the second alignment</u> target <u>which</u> has a width that corresponds to a stepper rotational error between the first region and an adjacent second region of the wafer.

- 2. (previously presented) The wafer as recited in Claim 1 wherein opposing sides of the first region are equal in length, and wherein an alignment target is located at each midpoint of a side of first region.
- 3. (previously presented) The wafer as recited in Claim 1 wherein an alignment target is located at each corner of the first region.
- 4. (original) The wafer as recited in Claim 1 wherein said alignment targets are formed according to a positive resist process.
- 5. (original) The wafer as recited in Claim 1 wherein said alignment targets are formed according to a negative resist process.
- 6. (canceled)

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7. (original) The wafer as recited in Claim 1 wherein each of said alignment targets comprise a plurality of rectangles.

8-20. (canceled)

21. (currently amended) A semiconductor structure, comprising:

a wafer;

a plurality of four-sided integrated circuit regions, separated by scribe lines disposed on a first surface of the wafer; and

at least one alignment target disposed in a first scribe line, the first scribe line being a common region between a first stepper shot and a second stepper shot;

wherein the second stepper shot overlays an alignment target on the at least one alignment target disposed in the first scribe line and the resulting overlay target has a width that corresponds to a stepper rotational error between the first stepper shot and the second stepper shot.